

IN THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the above-referenced application:

1. (Canceled)
2. (Currently amended) The device of claim 1, wherein the etching process comprises at least one of wet etching and reactive ion etching.
3. (Original) The device of claim 2, wherein the wet etching comprises anisotropic etching.
4. (Currently amended) The device of claim 1, wherein at least a portion of at least one perimeter edge of the integrated circuit die is beveled by forming one or more v-shaped grooves in an upper surface of the device.
5. (Currently amended) The device of claim 1, wherein the angle of the upper surface of the at least one chamfer in the integrated circuit die is controlled, at least in part, by selectively varying one or more characteristics of the etching process.
6. (Original) The device of claim 5, wherein the one or more characteristics of the etching process comprises at least one of a type of etchant, a temperature and a duration of etching.
7. (Currently amended) The device of claim 1, further comprising a plurality of integrated circuit die, at least one of the integrated circuit die being separated from the semiconductor device by: (i) forming one or more v-shaped grooves in an upper surface of the device, the v-shaped grooves defining perimeter edges of the at least one integrated circuit die; and (ii) removing a back surface of the semiconductor device opposite the upper surface of the device

until at least a portion of the v-grooves are exposed; wherein a sidewall of each of the v-shaped grooves forms a beveled perimeter edge of the separated die.

8. (Canceled)

9. (Currently amended) The device of claim + 25, wherein the integrated circuit die comprises a plurality of chamfers, each of the chamfers joining a respective pair of adjacent sides of the integrated circuit die and having an upper surface which is angled relative to the respective pair of adjacent sides.

10. (Previously presented) The device of claim 9, wherein the respective angles of the upper surfaces of the chamfers relative to corresponding pairs of adjacent sides of the integrated circuit die are substantially matched to one another.

11. (Currently amended) The device of claim + 25, wherein the angle of the upper surface of the at least one chamfer in the integrated circuit die is substantially matched to an angle of a sidewall of a die collet configurable for receiving the die.

12. (Currently amended) The device of claim + 25, wherein at least two perimeter edges of the integrated circuit die are beveled by the etching process.

13. (Currently amended) The device of claim + 25, wherein all perimeter edges of the integrated circuit die are beveled by the etching process.

14. (Previously presented) A method for separating at least one integrated circuit die from an associated semiconductor wafer, the method comprising the steps of:

forming one or more v-shaped grooves in an upper surface of the semiconductor wafer by an etching process, the one or more v-shaped grooves defining perimeter edges of the at least one integrated circuit die;

removing a back surface of the semiconductor wafer opposite the upper surface of the wafer until at least a portion of the one or more v-shaped grooves are exposed; and

forming at least one chamfer in the at least one integrated circuit die, the chamfer extending from a top surface of the integrated circuit die to an intersection of first and second adjacent sides of the at least one integrated circuit die, the chamfer having an upper surface which is angled relative to the first and second adjacent sides;

wherein a sidewall of each of the one or more v-grooves forms a beveled perimeter edge of the separated at least one integrated circuit die.

15. (Original) The method of claim 14, wherein the etching process comprises anisotropic etching.

16. (Previously presented) The method of claim 14, further comprising the step of controlling an angle of at least one of the upper surface of the chamfer and the sidewall of at least one of the v-shaped grooves, at least in part, by selectively varying one or more characteristics of the etching process.

17. (Previously presented) The method of claim 16, wherein the one or more characteristics of the etching process comprises at least one of a type of etchant, a temperature and a duration of etching.

18. (Currently amended) A method for reducing post-fabrication surface damage to an integrated circuit die, the method comprising the step of forming at least one chamfer in the integrated circuit die using an etching process, the chamfer extending from a top surface of the integrated circuit die to an intersection of first and second adjacent sides of the integrated circuit

die, the chamfer having an upper surface which is angled relative to the first and second adjacent sides, a first perimeter edge of the chamfer being formed by the first side of the integrated circuit die, a second perimeter edge of the chamfer being formed by the second side of the integrated circuit die, and a third perimeter edge of the chamfer being formed by an upper surface of the integrated circuit die, so that the upper surface of the chamfer is substantially triangular in shape.

19. (Previously presented) The method of claim 18, further comprising the step of controlling an angle of the upper surface of the at least one chamfer by selectively varying one or more characteristics of the etching process.

20. (Previously presented) The method of claim 18, wherein the step of forming the at least one chamfer comprises forming one or more v-shaped grooves in an upper surface of the integrated circuit die.

21. (Previously presented) The method of claim 18, wherein the step of forming the at least one chamfer comprises the step of substantially matching the angle of the upper surface of the chamfer to an angle of at least one sidewall of a die collet configurable for receiving the die.

22. (Currently amended) A packaged integrated circuit device, comprising:

at least one integrated circuit die, the at least one integrated circuit die having at least one chamfer extending from a top surface of the integrated circuit die to an intersection of first and second adjacent sides of the at least one integrated circuit die, the chamfer having an upper surface which is angled relative to the first and second adjacent sides, the chamfer being formed by an etching process;

wherein a first perimeter edge of the chamfer is formed by the first side of the integrated circuit die, a second perimeter edge of the chamfer is formed by the second side of the integrated circuit die, and a third perimeter edge of the chamfer is formed by an upper surface of

the integrated circuit die, so that the upper surface of the chamfer is substantially triangular in shape.

23. (Previously presented) The device of claim 22, wherein at least a portion of at least one perimeter edge of the at least one integrated circuit die is beveled by forming one or more v-shaped grooves in an upper surface of the at least one integrated circuit die.

24. (Previously presented) The device of claim 22, wherein the angle of the upper surface of the chamfer in the at least one integrated circuit die is controlled, at least in part, by selectively varying one or more characteristics of the etching process.

25. (Previously presented) A semiconductor device, comprising:

an integrated circuit die, the integrated circuit die having at least one chamfer joining first and second adjacent sides of the integrated circuit die, the chamfer having an upper surface which is angled relative to the first and second adjacent sides, the chamfer being formed by an etching process;

wherein a first perimeter edge of the chamfer is formed by the first side of the integrated circuit die, a second perimeter edge of the chamfer is formed by the second side of the integrated circuit die, and a third perimeter edge of the chamfer is formed by an upper surface of the integrated circuit die, so that the upper surface of the chamfer is substantially triangular in shape.